Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

CLAIMS LISTING (all of presented claims 1-44)

CLAIM 1 (*Original*): A contentions avoiding method for allowing an independently-clocked job requestor to request respective processing of respectively requested jobs in an independently clocked, job processor where variable communication latencies may exist between the job requestor and the job processor, said method being machine implemented and comprising:

(a) issuing to the job requestor, a first time stamp representing a respectively scheduled, first time within a timing reference frame of the job processor at which a respective first job is to be performed;

(b) in response to receipt of the first time stamp, sending from the job requestor to the job processor, a combination of job payload data and a second time stamp also representing the scheduled, first time;

(c) in response to receipt by the job processor of the combination of the job payload data and the second time stamp, storing the received job payload data in the job processor; and

(d) causing the job processor to process the stored payload data when a time corresponding to the second time stamp occurs within the timing reference frame of the job processor.

CLAIM 2 (Canceled).

CLAIM 3 (*Original*): A data sets re-ordering method for returning to a pre-established order and on-the-fly, data sets which are transmitted from different source units, over a distributed interconnect and processed within a distributed processing fabric and after said processing, transmitted to a common destination unit, where different parts of the distributed interconnect are subject to respectively different or variable communication latencies, said re-ordering method being machine implemented and comprising:

(a) associating with each transmitted data set a respective source indicator, a logical sequence indicator, and a process scheduling time stamp;

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(b) within the distributed processing fabric, processing each transmitted data set at a respective local time of the distributed processing fabric, where the respective local time for processing is identified by the process scheduling time stamp of the respective, transmitted data set; and

(c) as source and sequence associated ones of the transmitted data sets arrive sequentially at the common destination unit, positionally swapping the sequentially arriving data sets on-the-fly and in accordance with their respective source and sequence indicators so as to bring data sets of respective sources into relative sequence with one another as specified by the sequence indicators of respective source units.

CLAIM 4 (*Currently Amended*): A distributed payload processing system comprising:

(a) a first circuit supporter having a respective first, independent clock, where the first circuit supporter is adapted to support a first set of one or more of job requestor units and job processor units, where said units of the first set are clocked by the first independent clock;

(b) a second circuit supporter having a respective second, independent clock, where the second circuit supporter is adapted to support a second set of one or more of job requestor units and job processor units, where said units of the second set are clocked by the second independent clock;

(c) an interconnect operatively coupling the first circuit supporter with the second circuit supporter such that job requestor units of one of the first and second circuit supporters can send to one or more job processor units in the other of said circuit supporters, requests for respective processings of job payloads which are to be later supplied from the corresponding job requestor units to the respective job processor units,

where in response to at least some of said sent requests, the respective job processor units send to the corresponding job requestor units corresponding grants, and

where variable latencies may exist within the interconnect for communications carried over the interconnect between the job requestor units and the job processor units, and

(c.1) said grants that are sent over the interconnect include respective time stamps representing respectively scheduled time slots within respective timing reference frames of the respective job processor units at which respective ones of requested processing jobs are to be performed in the grant-giving job processor units.

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CLAIM 5 (*Original*): A scheduling support subsystem for enabling scheduling of payload processing actions in a request/grant system where effective latency between grant release and completed arrival in a payload processing unit of a corresponding payload can vary as a function of one or more latency factors in the group consisting of: (1) respective locations of payload source and payload processing units, (2) temperature, (3) time, (4) clock frequency and/or clock phase differences, (5) interconnect link lengths between respective points of grant release and respective points of payload arrival, and (6) local synchronization window lengths and/or phases at the respective locations of payload source and payload processing units; where the scheduling support subsystem comprises:

(a) a grant stamper for stamping released grants with respective time markers representing corresponding time points in a time frame of the payload processing unit, said represented time points being when the payloads corresponding to the released grants are to be processed by the payload processing unit; and

(b) latency fixing means for fixing latency between grant release and time of payload processing in the payload processing unit essentially to a predefined round-trip value.

CLAIM 6 (*Original*): The scheduling support subsystem of **Claim 5** wherein:

(b.1) the predefined round-trip value is at least greater than the average of non anomalous ones of said effective latencies between the grant releases and the completed arrivals of the corresponding payloads in the system.

CLAIM 7 (*Original*): The scheduling support subsystem of **Claim 5** wherein:

(b.1) the predefined round-trip value is at least as great as the maximum, non-infinite and non anomalous one of said effective latencies between the grant releases and the completed arrivals of the corresponding payloads in the system.

CLAIM 8 (*Original*): The scheduling support subsystem of **Claim 5** wherein the latency fixing means includes:

(b.1) an alignment queue provided in the payload processing unit for delaying the processing of received payloads to respective local times corresponding with payload stamps accompanying the received payloads, where the payload stamps correspond to the time markers stamped by the grant stamper.

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CLAIM 9 (*Original*): The scheduling support subsystem of **Claim 8** wherein the latency fixing means includes:

(b.2) delay adjusting means for adjusting said essentially fixed latency between grant release and time of payload processing in the payload processing unit.

CLAIM 10 (*Original*): The scheduling support subsystem of **Claim 5** wherein the latency fixing means includes:

(b.1) a local time defining means provided in the payload processing unit for defining when in a local time frame of the payload processing unit said corresponding time points occur, where the time points correspond to the time markers stamped by the grant stamper.

CLAIM 11 (*Original*): The scheduling support subsystem of **Claim 10** wherein:

(a.1) the grant stamper includes a first sequencer which sequences through a first wraparound sequence of markers that respectively represent said corresponding time points in the time frame of the payload processing unit; and

(b.1a) the local time defining means includes a second sequencer, that is operatively coupled to the first sequencer and that sequences through the first wraparound sequence of markers while lagging behind said sequencing of the first sequencer by a configurable lag factor, where said configurable lag factor can vary at least as much as can; for respective grant-carrying links and payload-carrying links of the system, the link-related latencies between the grant releases and the completed arrivals of the corresponding payloads on respective interconnect links in the system so that, given an actual latency with its corresponding variance for a corresponding grant-carrying link and a corresponding payload-carrying link, the sum of time spent sitting in an alignment queue by a given, arrived payload and of the actual latency experienced by that payload defines said, essentially fixed latency value.

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CLAIM 12 (*Original*): The scheduling support subsystem of **Claim 11** wherein:

(a.1a) the first sequencer is clocked independently of the second sequencer.

CLAIM 13 (*Original*): The scheduling support subsystem of **Claim 12** wherein:

(b.1b) the variable lag factor between the first and second sequencers is determined from test transmissions sent from a respective locale of one of the first and second sequencers to a respective other locale of another of the first and second sequencers by way of different ones of interconnect link lengths provided between a respective point of grant release and respective points of payload arrival.

CLAIM 14 (*Original*): A clock-tree free, scalable system for moving payload signals from respectively-clocked source circuits and through an independently-clocked, payload-processing layer for subsequent delivery to respectively-clocked destination circuits without need for a clock tree extending between the payload-processing layer and either of the source or destination circuits, where said destination circuits may include said source circuits or other respectively-clocked ones of the destination circuits; where a source-to-processing-to-destination interconnect is provided for transmitting payload signals, request and corresponding grant signals, and other signals between the source circuits, the payload-processing layer, and the destination circuits, and where said interconnect can exhibit different signals transmission latencies between various ones of the source circuits, different processing parts of the payload-processing layer, and the destination circuits; said scalable system comprising:

(a) grant stamping units for stamping respective grant signals each with a grant time stamp that indicates when, within a respective time frame of a corresponding, processing part of the payload-processing layer, processing is to take place for a payload signal corresponding to the stamped grant signal;

(b) alignment queues provided adjacent to corresponding ones of the payload-processing parts of the payload-processing layer, for storing respective payload signals received by the payload-processing parts prior to processing times indicated by respective ones of the grant time stamps; and

(c) process coordinating means, operatively coupled to the alignment queues and responsive to the grant time stamps or stamp signals derived therefrom, for controlling which of the payload signals stored in the alignment queues will be processed by which of the payload-processing parts and when, in accordance with the processing times indicated by respective ones of the grant time stamps or said stamp signals derived therefrom.

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CLAIM 15 (*Original*): The scalable system of **Claim 14** wherein each grant stamping unit includes:

(a.1) a grant time counter that sequences through a wrap-around series of states that represent grantable processing time slots in a corresponding payload-processing part, where the grant time counter is clocked by a local timing generator of the grant stamping unit; and

(a.2) a grant source queue for storing grant identification information indicating for respective ones of the grantable processing time slots at least whether a valid grant signal was issued with a corresponding grant time stamp for that grantable processing time slot or at least which of said plural align queues a corresponding payload signal is to be acquired from for processing during that grantable processing time slot.

CLAIM 16 (*Original*): The scalable system of **Claim 14** wherein for each of the alignment queues said scalable system includes:

(b.1) popping means for popping from a respective one of the alignment queues, at or just before the occurrence of a granted, processing time slot, the corresponding payload signal of that granted, processing time slot so that the popped payload signal can be duly processed during the granted, processing time slot by the corresponding payload-processing part.

CLAIM 17 (*Original*): The scalable system of **Claim 16** wherein for each of the alignment queues said scalable system further includes:

(b.2) pushing means for pushing into an unused storage space of a respective one of the alignment queues, and before the occurrence of a granted, processing time slot, the corresponding payload signal of that granted, processing time slot so that the pushed payload signal can be later popped and duly processed during the granted, processing time slot by the corresponding payload-processing part.

CLAIM 18 (*Original*): The scalable system of **Claim 17** wherein each pushing means includes:

(b.2a) null dropping means which excludes from said pushing into unused storage space, data of a received payload signal if the received payload signal is indicated to be invalid.

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CLAIM 19 (*Original*): The scalable system of **Claim 17** wherein each of the alignment queues said scalable system further includes:

(b.3) latency determining means, coupled to the pushing means and to the popping means, for determining what relative latency separates currently popped payloads from currently pushed payloads and for outputting a signal representing that relative latency.

CLAIM 20 (*Original*): The scalable system of **Claim 19** and further comprising:

(b.4) latency evaluating means, coupled to a plurality of said latency determining means of a respective plurality of the alignment queues, the latency evaluating means being for evaluating the relative latency output signals of said plurality of latency determining means and for determining whether corrective action needs to be taken if all or a subset of said relative latency output signals indicate respective relative latencies outside of predefined bounds established for such relative latencies.

CLAIM 21 (*Original*): The scalable system of **Claim 14** wherein said payload-processing parts each includes a payload switching matrix.

CLAIMS 22-35 (*Canceled*).

CLAIM 36 (*Previously Presented*): An expandable digital system to which independently-clocked data-sourcing circuits and/or independently-clocked data-processing circuits can be added without keeping all parts the expanded system synchronized to a common seed clock, said expandable digital system comprising:

(a) a time-stamp output and recovery mechanism which outputs for a first data-processing circuit that is to process first input data at a prescheduled time within a time frame of the first data-processing circuit, a first time-stamp signal for transmission to a supplier of said first input data, the output first time-stamp signal representing the prescheduled time within said time frame and which recovers a corresponding second time-stamp signal together with said first input data from said supplier, the recovered second time-stamp signal also

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representing the prescheduled time within said time frame at which the recovered first input data is to be processed by the first data-processing circuit; and

(b) a rate-creep preventing mechanism distributed among the independently-clocked data-sourcing circuits and independently-clocked data-processing circuits of said expandable digital system for preventing faster paced ones of the independently-clocked circuits from outpacing slower ones of the independently-clocked circuits over a relatively long term of operation even if clock paces of the independently-clocked circuits are relatively close to one another.

CLAIM 37 (*Previously Presented*): The expandable digital system of Claim 36 wherein:

(b.1) said rate-creep preventing mechanism includes a static link-rate constraining mechanism.

CLAIM 38 (*Previously Presented*): The expandable digital system of Claim 37 wherein:

(b.1a) said static link-rate constraining mechanism includes an idle bite inserter.

CLAIM 39 (*Previously Presented*): The expandable digital system of Claim 36 wherein:

(b.1) said rate-creep preventing mechanism includes a dynamic link-rate adjusting mechanism.

CLAIM 40 (*Previously Presented*): The expandable digital system of Claim 39 wherein:

(b.1a) said dynamic link-rate adjusting mechanism includes a generator of a back pressure indicator.

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CLAIM 41 (*Currently Amended*): A method of expanding size of a digital system without keeping all parts the expanded system synchronized to a common seed clock, said method comprising:

(a) adding an independently-clocked data-sourcing circuit to the system where the data-sourcing circuit sends requests to one or more other parts of the system for processing of data sourced by the data-sourcing circuit;

(b) causing the system to respond to processing requests sent by the added-on, data-sourcing circuit with corresponding grant signals, where the grant signals include one or more time stamps indicating a time point with a timing frame of processing part of the system that the processing part is scheduled to process the data sourced by the data-sourcing circuit.

CLAIM 42 (*Currently Amended*): The expansion method of Claim 41 wherein:

(a.1) said adding ~~*includes*~~ is constituted by adding a single new circuit board to the system, where the added independently-clocked data-sourcing circuit resides on the new circuit board.

CLAIM 43 (*Currently Amended*): A method of expanding size of a digital system without keeping all parts the expanded system synchronized to a common seed clock, said method comprising:

(a) adding an independently-clocked data-processing circuit to the system where the data-processing circuit receives requests from one or more other parts of the system for processing of data sourced by data-sourcing circuits within the system;

(b) causing the added-on data-processing circuit to respond to processing requests received from the one or more other parts of the system by outputting corresponding grant signals, where the grant signals include one or more time stamps indicating a time point with a timing frame of the added-on data-processing circuit when the system sourced data is scheduled to be processed by the added-on data-processing circuit.

CLAIM 44 (*Currently Amended*): The expansion method of Claim 43 wherein:

(a.1) said adding ~~*includes*~~ is constituted by adding a single new circuit board to the system, where the added independently-clocked data-processing circuit resides on the new circuit board.

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